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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/677,392	09/29/2000	Aditya Mukherjee	042390.P9572	3111

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EXAMINER	
CHAUDRY, MUJTABA M	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 10/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/677,392	MUKHERJEE, ADITYA	
	Examiner	Art Unit	
	Mujtaba K. Chaudry	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-10,12-20,22 and 23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-10,12-20,22 and 23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Applicant's arguments with respect to pending claims 1, 3-10, 12-20, 22 and 23 filed August 25, 2005 have been fully considered but are not persuasive. The Examiner would like to point out that this action is made final (See MPEP 706.07a).

Applicant contends, "...Wasson does not teach or suggest an integrated circuit to include a test controller etc..." The Examiner respectfully disagrees. In Figure 1 along with associated text, col. 3, lines 54-55, Wasson teaches an **integrated circuit tester 10** which includes the tester as well as the device under test.

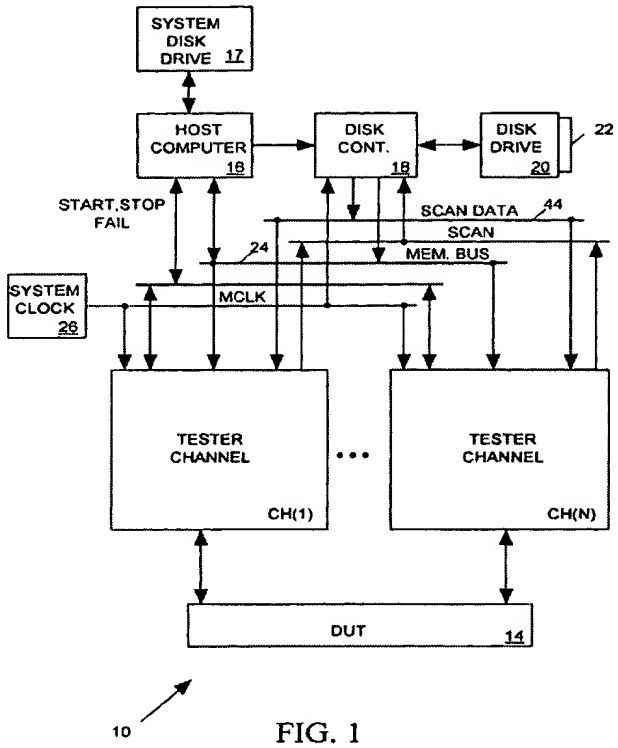

FIG. 1

However, even if the tester was integrated into the circuit or external to the circuit, it does not render the method and apparatus patentably distinct. The Examiner would like to point out that built-in self-testing is a well know procedure within the art of testing integrated circuits and is a obvious engineering design choice. See *In re Larson 144 USPQ 347* (CCPA 1965).

Applicant contends, "...Wasson does not even use the term packet in the entire reference..." The Examiner respectfully agrees with the Applicant. However, the Examiner would like to point out that digital data is transmitted in the form of packets. Therefore Wasson teaches to transmit data in packets.

The Examiner disagrees with the Applicant and maintains rejections with respect to pending claims 1, 3-10, 12-20, 22 and 23. All arguments have been considered. It is the Examiner's conclusion that pending claims 1, 3-10, 12-20, 22 and 23 are not patentably distinct or non-obvious over the prior art of record. See office action:

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, 3-10, 12-20 and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wasson (USPN 6181151 B1). See prior office action:

As per claims 1, 18 and 22-23, Wasson substantially teaches (title and abstract) an integrated circuit tester with a plurality of tester channels for testing a device under test. The tester channels include an instruction memory for storing a set of test instructions which are executed during testing. Wasson teaches the test instructions to include a vector data which indicates a particular test and other instructions which direct a certain number of data bits to the tester. Wasson teaches (Figure 1 and col. 4, lines 17-54) a host computer which signals a disk controller to read the instructions for the tester channel and write those instructions onto an instruction memory—analogous to memory chip in the present application. The examiner would like to point out that the test controller in the present application is analogous to the disk controller of Wasson, since the test controller (in the present application) is defined to be any device that asserts test instructions (present application: specification page 6, lines 13-17). A test bus is shown in figure 1 (Wasson) that is connected to the test controller/disk controller and the logic unit control. The logic unit controller/deskew controller in the present application is analogous to the timing circuit of Wasson, since the logic unit controller/deskew controller is defined to synchronize the instructions (present application: specification pages 7-8, lines 28 and 1-5 respectively). As regards to the "design" limitation of the present application, Wasson teaches (col. 4, line 30) logic test activities that include various designs. As a note of reference the "design" limitation is also rejected above under 35 USC 112, 2nd paragraph for being indefinite. Wasson teaches (col. 4, lines 17-21) the tester to be adapted to test programmable logic devices which is analogous to logic unit in the present application.

Wasson does not explicitly teach the external device to comprise of a keyboard, mouse and a modem as stated in the present application.

However, Wasson teaches a host computer (figure 2) which is used as control means for the testing apparatus. Specifically, Wasson teaches (col. 4, lines 31-45) the tester to include a host computer which is signals the disk controller to read and write instructions to the instruction memory. Furthermore, the examiner would like to point out that a host computer is defined (The Authoritative Dictionary of IEEE Standard Terms, 7th ed.) to be a computer attached to a network providing primary services such as computation, data base access, special programs or programming languages which may have multiple processing elements (i.e. keyboard, mouse, etc).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate a keyboard, modem and a mouse within the system of Wasson as stated in the present application. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill would have recognized that a host computer might inherently include a keyboard, mouse and modem for communicating with a testing apparatus which would also abate complications involved.

As per claims 5-9, 13-17 and 19-20, Wasson substantially teaches, in view of above rejections, (col. 5, lines 55-68—col. 6, lines 1-42) a set of instruction bits and an instruction memory register as stated in the present application. Specifically, Wasson teaches to supply the instructions to each channel CH(1)-CH(N) before testing and supplying scan data (analogous to ancillary data in the present application) to various channels during a test. Before the start of the test the disk controller reads the channel instructions and writes them into the instruction

memory of each channel. The disk controller also reads control data for each channel out of disk and writes that control data into a set of addressable control registers within the channel via memory bus and memory controller. The control data stored in addressable control registers tells shift register which M bits of the 12-bit scan data word that it is to shift in. If the channel is the only channel using scan data during a test M is 12 and the channels' shift register shifts in all 12 bits of scan data in response to each SHIFT_IN signal pulse. For example if four channels use scan data during a test, the control data tells the shift register of each channel to shift in a particular set of three of the 12 scan data bits. The control data also tells state machine how many scan bits are being shifted in so that state machine knows how many test cycles to wait between successive SHIFT_IN pulses. Wasson teaches (figure 2) a state machine that is analogous to the finite state machine in the present application.

Wasson does not explicitly teach a test bus to include n number of lines such that "$n = a + \log_2 i$" wherein "n" is defined to be the number of lines, "a" is defined to be number of ancillary transmission bits and "$\log_2 i$" is defined as the number of instruction bits as stated in the present application.

However, the examiner would like to point out that Wasson does teach a process that is similar and essentially includes this variation. Specifically, Wasson teaches (col. 6, lines 43-67) to supply control instructions and scan data (analogous to ancillary transmission bits) to each channel before testing. Furthermore the control data determines what number of M bits of the 12-bit scan word will be sent and also how the encoder converts the scan data. The control data also determines tells state machine (analogous to finite state machine in the present application) how many scan bits are being shifted in so that state machine knows how many test cycles to wait

between successive SHIFT_IN pulses (analogous to clock signal for the ancillary transmission bits in the present application).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention was made to define the design parameters of Wasson by setting them in accordance to the equation "$n = a + \log_2 i$" wherein "n" is defined to be the number of lines, "a" is defined to be number of ancillary transmission bits and "$\log_2 i$" is defined as the number of instruction bits as stated in the present application. This modification would have obvious to one of ordinary skill in the art because one of ordinary skill would have recognized that the equation "$n = a + \log_2 i$" (wherein "n" is defined to be the number of lines, "a" is defined to be number of ancillary transmission bits and "$\log_2 i$" is defined as the number of instruction bits) is an obvious design choice that one is entitled to in the making of the method and apparatus. Furthermore, the examiner would like to point out that there are several ways to state a limitation mathematically, which essentially holds the same underlying meaning.

As per claims 3-4, 10 and 12, Wasson substantially teaches, in view of above rejections, an integrated circuit tester with a plurality of tester channels for testing a device under test. The tester channels include an instruction memory for storing a set of test instructions which are executed during testing. Wasson teaches the test instructions to include a vector data which indicates a particular test and other instructions which direct a certain number of data bits to the tester. Wasson teaches (Figure 1 and col. 4, lines 17-54) a host computer which signals a disk controller to read the instructions for the tester channel and write those instructions onto an instruction memory—analogous to memory chip in the present application. The examiner would like to point out that the test controller in the present application is analogous to the disk

controller of Wasson, since the test controller (in the present application) is defined to be any device that asserts test instructions (present application: specification page 6, lines 13-17). A test bus is shown in figure 1 (Wasson) that is connected to the test controller/disk controller and the logic unit control. The logic unit controller/deskew controller in the present application is analogous to the timing circuit of Wasson, since the logic unit controller/deskew controller is defined to synchronize the instructions (present application: specification pages 7-8, lines 28 and 1-5 respectively). As regards to the "design" limitation of the present application, Wasson teaches (col. 4, line 30) logic test activities that include various designs. As a note of reference the "design" limitation is also rejected above under 35 USC 112, 2nd paragraph for being indefinite. Wasson teaches (col. 4, lines 17-21) the tester to be adapted to test programmable logic devices which is analogous to logic unit in the present application.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiries concerning this communication should be directed to the examiner, Mujtaba Chaudry who may be reached at 571-272-3817. The examiner may normally be reached Mon – Thur 6:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Albert DeCady at 571-272-3819.

Mujtaba Chaudry
Art Unit 2133
September 27, 2005

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100